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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,992	03/17/2004	Hiroshi Matsushita	03180.0357	3342

22852 7590 11/15/2007

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP
901 NEW YORK AVENUE, NW
WASHINGTON, DC 20001-4413

EXAMINER	
STEVENSON, ANDRE C	

ART UNIT	PAPER NUMBER
2812	

MAIL DATE	DELIVERY MODE
11/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/801,992	MATSUSHITA ET AL.	
	Examiner	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *17 and 18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 14-16* is/are rejected.

7)☒ Claim(s) *13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/25/06,03/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 06/06/05 and 12/22/05 were filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims #1 and 16 are drawn to a method for inspecting LSI's, classified in class 438, subclass 4.

II. Claims #17-20, drawn to a defect inspection data analysis apparatus, classified in class 257, subclass 765.

Inventions Group I and Group II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another and materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the method claimed by Group I can be inspected by an entirely different apparatus than that claimed in Group II.

During a telephone conversation with David Longo on October 23, 2007 a provisional election was made without traverse to prosecute the invention of Group I, claims #1-16. Affirmation of this election must be made by applicant in replying to this Office action. Claims

#17 and 18 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims **#1-7, 9-12 and 14-16** are rejected under 35 U.S.C. 102(e) as being unpatientable by Thanaka et al. (U.S. Pub. No.20030054573, Pub. Date 03/20/03, Filed 08/30/02).

Thanaka substantially shows the claimed invention, as shown in figures 1-20 and corresponding text, in a method for testing semiconductor parts, **pertaining to claim #1**, a method for analyzing fail bit maps comprising: inputting positions of failures in wafers; preparing sections on the wafers; calculating feature amounts configured to represent distributions of the failures in the wafers for each of the sections by at least one numerical value**(page #1, paragraph 0013)**; calculating a first numerical value configured to represent a degree of similarity between the feature amounts of the wafers **(page #4, paragraph 0063-0066; page #6, paragraph 0080)**; and detecting another wafer having the first numerical value greater than a predetermined first threshold for each of the wafers, and forming similar wafer groups of the wafers having the distributions of the

failures similar to each other **(page #4, paragraph 0067; page #5, paragraph 0071; page #6, paragraph 0077-0078).**

Pertaining to claim #2, Thanaka shows a method further comprising: finding another similar wafer group having a first ratio of the number of the wafers included in both of said another similar wafer group and each one of the similar wafer groups to the number of the wafers included in at least one of said another similar wafer group and the each one of the similar wafer groups to be equal to or greater than a predetermined second threshold; and configuring a first failure category from the similar wafer groups and another similar wafer group found for the each one of the similar wafer groups in decreasing order of the number of the wafers included in the similar wafer groups **(page #6, paragraph 0077-0079; page #7, paragraph 0086).**

Pertaining to claim #3, Thanaka shows, a method further comprising: determining the first failure category to which each of the wafers belong **(page #7, paragraph0088; page #7, paragraph 0086).**

Pertaining to claim #4, Thanaka shows, a method further comprising: identifying at least one of a manufacturing step and a manufacturing device configured to be commonly used to manufacture the wafers belonging to the first failure category from a process history **(abstract; page #1, paragraph 0001; page #6, paragraph 0080-0083).**

Pertaining to claim #5, Thanaka shows a method wherein calculating the feature amounts includes calculating a failure existing rate as a ratio of the number of the failures developed within each of the sections to the number of all of the failures **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080).**

Pertaining to claim #6, Thanaka shows, a method wherein calculating the feature amounts includes calculating a first autocorrelation function with an exposure cycle period as a lag for each of the sections **(page #3, paragraph 0053-0055; page #9, paragraph 0103).**

Pertaining to claim #7, Thanaka shows a wherein calculating the feature amounts is by expanding the sections and calculating the feature amounts by using the number of the failures developed in the sections **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080).**

Pertaining to claim #9, Thanaka shows, a method further comprising: storing an alignment order for the feature amounts and a lag width; aligning the feature amounts as waveforms based on the alignment order for each of the wafers; and calculating second autocorrelation coefficients of the waveforms based on the lag width **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080).**

Pertaining to claim #10, Thanaka shows, a method further comprising: setting a second ratio of the number of the wafers belonging to the first failure category and having the first numerical value equal to or greater than the first threshold to the number of the wafers belonging to the first failure category, and setting a zero value when each of the wafers fail to belong to the first failure category, to each of the wafers as representative lot values of lots configured with the wafers; calculating a second numerical value configured to represent the degree of similarity between the representative lot values of the lots ; and detecting another lot having the second numerical value greater than a predetermined third threshold for each of the lots, and forming similar lot sets of the lots having development tendencies of the failures similar

to each other **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080; page #7, paragraph 0086).**

Pertaining to claim #11, Thanaka shows, a method further comprising: finding another similar lot set, which allows a third ratio of the number of the lots included in both of said another similar lot set and one of the similar lot sets to a number of the lots included in at least one of said another similar lot set and one of the similar lot sets to be equal to or greater than a predetermined fourth threshold; configuring a second failure category from the similar lot sets and the another similar lot set, which is found for the similar lot sets, in decreasing order of the number of the lots included in the similar lot sets; and determining a representative lot value that is most characteristic in the second failure category **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080; page #7, paragraph 0086).**

Pertaining to claim #12, Thanaka shows, a method further comprising: aligning the representative lot values for each of the lots in one of a decreasing and increasing order of the representative lot values, so as to form a reference waveform; and calculating a residual sum of squares between a waveform, which is formed by aligning the representative lot values of other lots in the decreasing or increasing order, and the reference waveform **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080; page #7, paragraph 0086).**

Pertaining to claim #14, Thanaka shows, a method wherein a overlapped area of the sections expanded and the sections adjacent to the sections expanded occupies 60% or less of an area of the sections **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080; page #7, paragraph 0086).**

Pertaining to claim #15, Thanaka shows, a method wherein setting as the representative lot values uses one of average lot values, a wafer failure rate per lot, the intra-lot maximum value, degree of even / odd-caused inhomogeneous distribution, degree of first / latter half-caused inhomogeneous distribution, degree of wafer number-caused inhomogeneous distribution, or a periodic regularity, for the second ratio **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080; page #7, paragraph 0086).**

Pertaining to claim #16, Thanaka shows, a method wherein determining the representative lot value includes: finding a first total sum of the second numerical values of the representative lot values of the lots belonging to the second failure category and a second total sum of the second numerical values when a single component is excluded from the representative lot values; and finding a component, which allows the difference between the first **(page #4, paragraph 0063-0067; page #5, paragraph 0071; page #6, paragraph 0077-0078, 0080; page #7, paragraph 0086).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim #8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thanaka et al. (U.S. Pub. No.20030054573, Pub. Date 03/20/03, Filed 08/30/02) as applied to claims **1-7, 9-12 and 14-16** above, and in view of Mansfield et al. (U.S. Pat. No.6,526,164 B1, Pat. Date 02/25/03, Filed 05/27/99).

Thanaka substantially shows the claimed invention, as shown in the previous rejection above.

Thanaka fails to show, **respect to claim #8**, a method further comprising: generating frequency distributions of the feature amounts for each of the wafers, approximating logarithms of the frequency distributions with quadratic functions, finding second-order coefficients and first-order coefficients of the quadratic functions, and determining whether there are clustering failures based on the second-order coefficients and the first-order coefficients.

Mansfield teaches, in a similar method for determining whether defects can be detected in photomask, ***pertaining to claim #8,*** a method comprising: generating frequency distributions of the feature amounts for each of the wafers, approximating logarithms of the frequency distributions with quadratic functions, finding second-order coefficients and first-order coefficients of the quadratic functions, and determining whether there are clustering failures based on the second-order coefficients and the first-order coefficients **(Column #7, lines 60-67; Column #8, lines 1-6).**

It would have been obvious to one having ordinary skill in the art at the time the invention was made, with respect to claim #8, to include a method comprising: generating frequency distributions of the feature amounts for each of the wafers, approximating logarithms

of the frequency distributions with quadratic functions, finding second-order coefficients and first-order coefficients of the quadratic functions, and determining whether there are clustering failures based on the second-order coefficients and the first-order coefficients, into the method of Thanaka, as taught by Mansfield, with the motivation that the quadratic functions yields very

Allowable Subject Matter

Claim#13 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim #13

- Performing Fourier transformation regarding the feature amounts as waveforms and comparing first spectra of Fourier transformation of the waveforms, and using a maximum entropy method

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

(703) 872-9306

Andre' Stevenson

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

10/26/07